LX1800

SMBus to Analog Interface

PRODUCTION DATA SHEET

DESCRIPTION

The LX1800 bridges the analog and digital world. The analog interface contains and eight bit ADC and 8 bit DAC and the digital interface is a serial data SMBus interface. The LX1800 works well in a feedback control system such as an LCD backlight system where the analog output of an ambient light sensor such as the LX1972 can be digitized allowing the micro controller to adjust the analog dimming signal accordingly.

The LX1800 has an internal bandgap reference and also allows the use of an external reference. The external reference can be used as an analog input for volume control using the DAC or to provide wider range for high amplitude analog signals.

The 8 pin MLP package is small occupying no more area than a TSOT package.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: http://www.microsemi.com

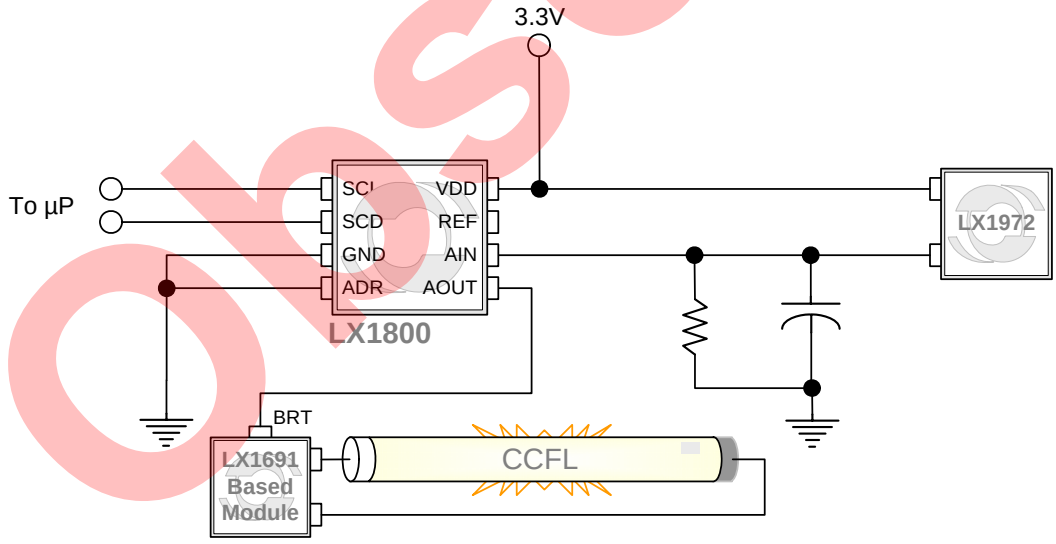
KEY FEATURES

- 8 bit accuracy
- ADC and DAC in one package
- Fully compliant to standard SMBus
- Bus controllable Sleep mode
- Optional external reference

APPLICATIONS

- Processor controlled dimming
- VID control interface
- Digital regulator control
- Audio volume control

PRODUCT HIGHLIGHT



PACKAGE ORDER INFO

T_J (°C)	LD	Plastic MLP 8-pin RoHS Compliant / Pb-free
-40 to +85		LX1800ILD

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. LX1800ILD-TR)

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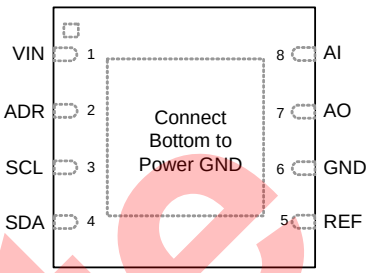
ABSOLUTE MAXIMUM RATINGS

Supply Input Voltage ..... -0.3V to 7.0V
REF, AO, AI, ADR, SCL, SDA ..... -0.3V to 7.0V
Operating Temperature Range ..... 150°C
Maximum Operating Junction Temperature ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Peak Package Solder Reflow Temp (40 second max. exposure) .... 260°C (+0, -5)

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

PACKAGE PIN OUT



LD PACKAGE
(Top View)

RoHS / Pb-free 100% Matte Tin Lead Finish

THERMAL DATA

LD **Plastic MLPD 8-Pin**

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	48°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

FUNCTIONAL PIN DESCRIPTION

Name	Description
ADR	SMBus Address – The address for the LX1800 is determined by the sate of this pin. ADR = GND is address 54B, ADR = VCC is address 55B.
AI	Analog Input – Sampled input for the Analog-to-Digital converter.
AO	Analog Output – Output of Digital-to-Analog converter.
GND	Ground – Connect to system ground.
REF	External Voltage Reference (optional) – Reference for both ADC and DAC. REF must be less than 80% of VIN.
SCL	SMBus Clock – Connect to SMBus Clock line
SDA	SMBus Data – Connect to SMBus Data line
VIN	Power Supply – Connect to a 2.7V to 5.5V power source.

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ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature -40°C ≤ T_A ≤ 85°C except where otherwise noted and the following test conditions: V_{CC} = 5V, V_{REF} external = 2.500V, Control register = 1BH.

Parameter	Symbol	Test Conditions	LX1800			Units
			Min	Typ	Max	
POWER SUPPLY						
Operating Supply Voltage	V_{CC}		2.7		5.5	V
Average Supply Current	I_{CC}	DAC = FFH; idle ADC		100	200	µA
Sleep Current	I_{CC}	Control Register = 10H			50	µA
DAC						
DAC Resolution				8		Bits
DAC Full-scale Output	V_{FS}	DAC = FFH; I_{AO} = 0 ± 10µA	2.42	2.50	2.58	V
DAC Zero-scale Output	V_{ZS}	DAC = 00H; I_{AO} = 0 ± 10µA	0		30	mV
DAC Absolute Accuracy		DAC = 00H to FFH	-5	0	-5	LSB
DAC Adjacent Code Error		DAC = 01H to FEH; GBNT	-0.5	0	0.5	LSB
DAC Transition Delay	T_{TD}	Delay from Stop Transition		1		µS
ADC						
Resolvable Input Range			0		5	V
ADC Mid point Output		V_{AI} = 1.25V	124	128	132	LSB
ADC Absolute Accuracy		V_{AI} = 0V to 2.5V	-6	0	6	LSB
Input Leakage Current	I_{AI}	V_{AI} = 1.25V	-3	0	3	µA
Input Capacitance	C_{AI}	V_{AI} = 1.25V		30		pF
Acquisition Time	T_{AQ}	V_{AI} = 1.25V		100	200	µs
EXTERNAL REF						
Input Range	V_{REF}		0		5	V
Input Leakage Current	I_{REF}		-50	0	50	nA
INTERNAL REF						
Reference Voltage	V_{INT}		1.96	2.00	2.04	V
ADR						
High Level Input Voltage	V_{AHL}		80			%VCC
Low Level Input Voltage	V_{ALL}				20	%VCC
Input Leakage Current	I_{ADR}		-50	0	50	nA
SCL, SDA						
High Level Input Voltage	V_{SHL}	2.7 ≤ V_{CC} ≤ 5.5V	2.1			V
Low Level Input Voltage	V_{SLL}	2.7 ≤ V_{CC} ≤ 5.5V			0.8	V
Input Leakage Current	I_{SMB}		-5	0	5	µA
SDA Low Level Output Voltage	V_{OL}	IOUT = 350µA			0.4	V
SMBUS						
SMB clock frequency	F_{CLK}		10		100	KHz

SMBUS COMMUNICATION FORMAT

The LX1800 looks for its unique address each time it detects a "start condition". If the address does not match, the LX1800 ignores all bus activity until it encounters another "start condition". If the address is a match, the LX1800 acknowledges that it has detected its address and a W/R bit to either read or write data. If the W/R bit is a "0", signifying a "write command", the next byte of data sent from the host will be the index. The index points to an internal register in the LX1800 that will be the object of the subsequent data transfers. There are four internal registers within the LX1800: The Control register, the DAC register ,the ADC register, and the MISC register. In a write command, the LX1800 will acknowledge the receipt of a valid index. After the index, there may be another byte of data; if so, this byte of data is loaded into the indexed register. The LX1800 will acknowledge receipt of the data byte. If the write command does not contain data, the command line will be terminated by a "stop condition" received from the host. If for some reason, the data transfer is corrupted prior to acknowledgement, the LX1800 will not acknowledge receipt of the byte in question and will not take action on the incomplete data. The LX1800 can receive only one data byte in a write command and will ignore all additional bus activity once it has acknowledged receipt of the data byte until the next "start condition" is detected. Receipt of a "stop condition" or "start condition" will reset the address detection state machine. The LX1800 does not support "Packet Error Code".

The host can read the contents of the indexed register within the LX1800 using a read command line. In this command line the W/R bit is set to "1". Upon receipt of a read command, the LX1800 will acknowledge that it has detected its address and a valid W/R bit; then it will put a copy of the one byte of data from the indexed register onto the bus. (As explained above, the index may be changed using a write command with or without an additional data byte.) Once the LX1800 has placed the byte of data on the serial bus, it will ignore all additional bus activity until the next "start condition" is detected.

Write Format (Two optional packet lengths)

Start	Address	W/R	Ack	Data	Ack	Stop
	0101100b or 0101101b	0		Index		

Start	Address	W/R	Ack	Data	Ack	Data	Ack	Stop
	0101100b or 0101101b	0		Index		1 byte Data		

Read Command Format:

Start	Address	W/R	Ack	Data	Ack	Stop
	0101100b or 0101101b	1		Read Indexed Register		

Repeated Start Command Format:

The LX1800 will support the execution of successive commands that are not separated by "stop conditions" provided the commands are otherwise formatted as indicated above.

GENERAL SMBUS PROTOCOL SUMMARY

(see SMBus specification version 2.0 for more details).

Start condition: Host sends a high-to-low SDA transition while SCL is high.

Address: Host sends to 0101100 ADR=GND; 0101101 ADR = VCC

W/R: Host sends a "Lo" bit for an instruction with a DATA Write and a "Hi" bit for a DATA Read.

Acknowledge: LX1800 and Host let SDA go high while SCL is low after data byte transfer indicating next byte may be sent.

Stop Condition: A low-to-high SDA transition while SCL is high.

Normal condition: SDA transitions only while SCL is low.

For timing information see SMBus specification version 2.0.

Data is transferred with the MSB first.

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SMBUS REGISTER MAP

Each register has an address which is programmed into the index register. The value in the index register determines which register is accessed on a given read or write operation.

Control Register:
Address = xxxxxx00b
Type = Read/Write
Default = 10000000
Bit Assignments:

7	Sleep Mode	1 = active mode, 0 = sleep mode
6	Reference	1 = external, 0 = internal
5	ADC Start	1 = start A/D; this bit is reset to 0 when conversion complete.
4	ADC Mode	1 = always on; 0 = turn on as required
3	Invert DAC Mode	1 = normal DAC bit polarity; 0 = inverted DAC input polarity
2	ADC Loop Back	1 = ADC drives DAC directly; 0 = DAC input comes from Bus
1	ADC Continuous	1 = ADC continuously converts; 0 = ADC on Bus command
0	ADC Clock Mode	1 = ADC uses SCL clock; 0 = ADC uses internal clock.

DAC Register:
Address = xxxxxx01b
Type = Read/Write
Default = 10000000b
Bit Assignments: FFh = full scale (VREF); 00h = 0V (normal polarity mode)

ADC Register:
Address = xxxxxx10b
Type = Read Only
Default = 00000000b
Bit Assignments: FFh = full scale (VREF); 00h = 0V

MISC Register:
Address = xxxxxx11b
Type = Read/Write for bits 7:4; Read Only for bits 3:0
Default = 00000101b
Bit Assignments:

7:4	Unassigned	
3:2	Version	01b = version 1
1:0	Revision	01b = revision 1

SIMPLIFIED BLOCK DIAGRAM

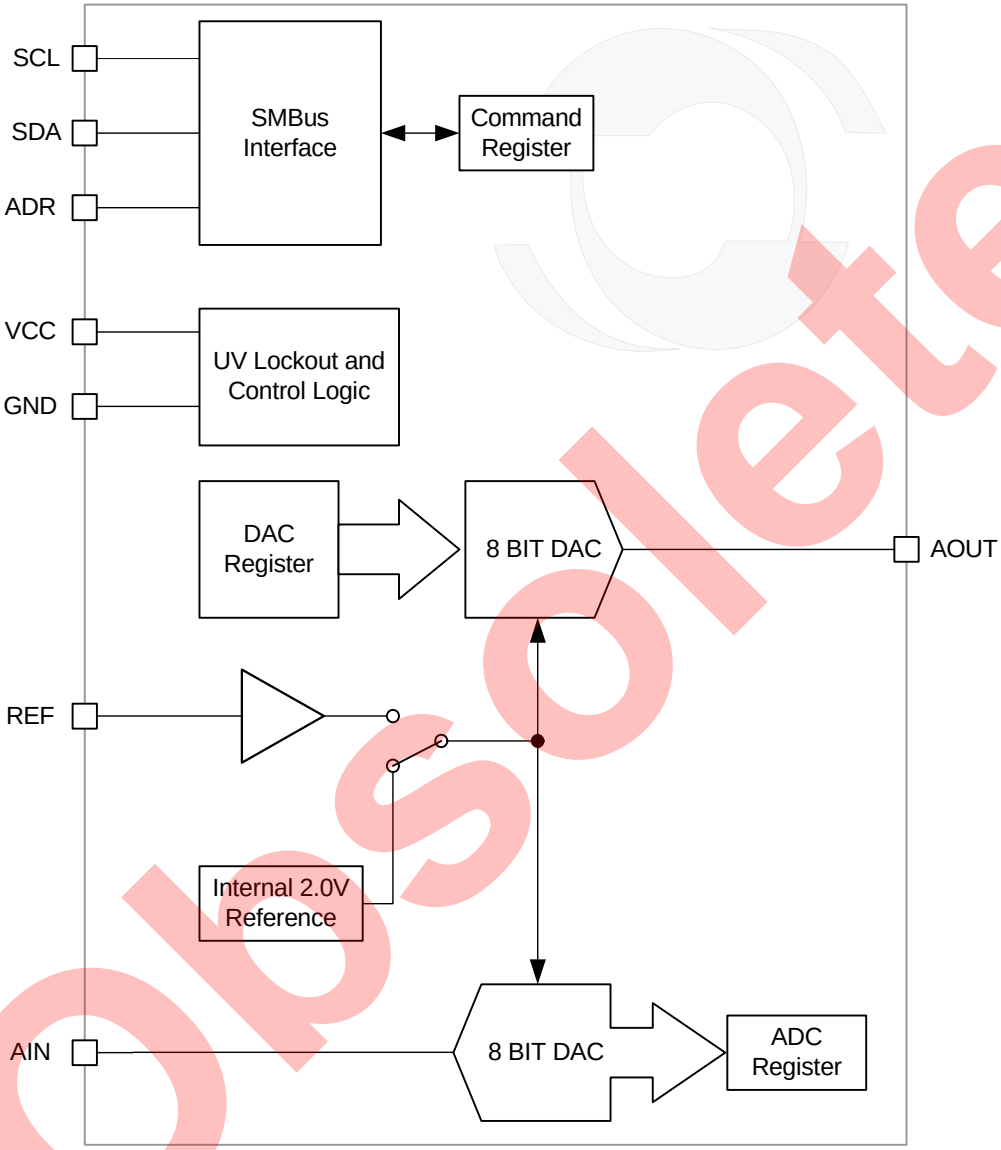

Figure 1 – Simplified Block Diagram

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APPLICATION CIRCUITS

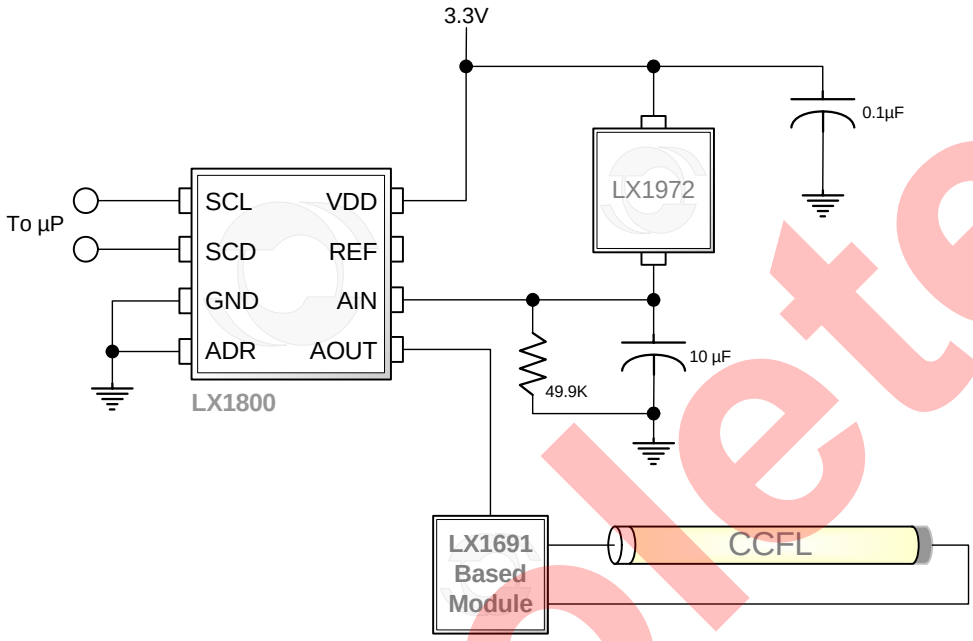

Figure 2 – Backlight dimmer with ambient light compensation

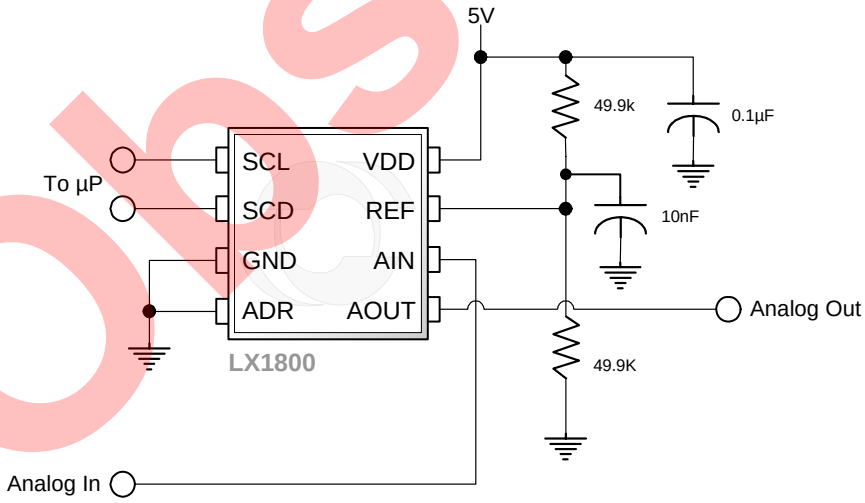

Figure 3 – 1) Log or exponential taper using a µP lookup table or 2) Infinite Sample and Hold.

APPLICATION CIRCUITS

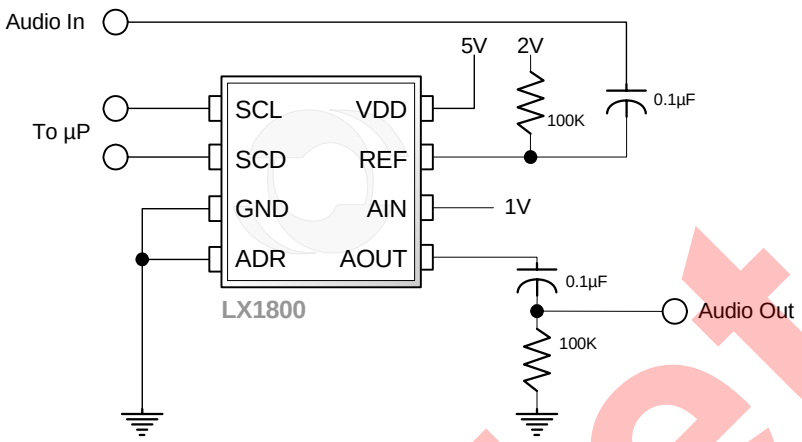

Figure 4 – Digital Volume Control with Audio Absent Detection.

THEORY OF OPERATION

BASIC FUNCTIONALITY

The LX1800 contains an 8 bit DAC, an 8 bit ADC and a SMBus interface which connects the input of the DAC and the output of the ADC to the SMBus host. The LX1800 contains an internal 2V reference and can also be configured to use an external reference. Since the 8 bit DAC is a multiplying type, the external reference can be used for an analog input for volume control applications. The ADC contains a sample and hold input that stores the analog voltage level while the conversion is being processed.

SMBUS INTERFACE

The LX1800 communicates over the SMBus in the slow speed Low Power Level and operates in a "slave" mode receiving commands and sending and receiving data from the host or bus "master". The LX1800 can be configured for one of two addresses, 0101100b when the ADR line is grounded and 0101101b when the ADR line is connected to Vcc.

The LX1800 has three internal registers, the Command register, the DAC register and the ADC register. The CMD register is read/write, the DAC register is write only and the ADC register is read only. Control of the LX1800 are performed through the CMD register.

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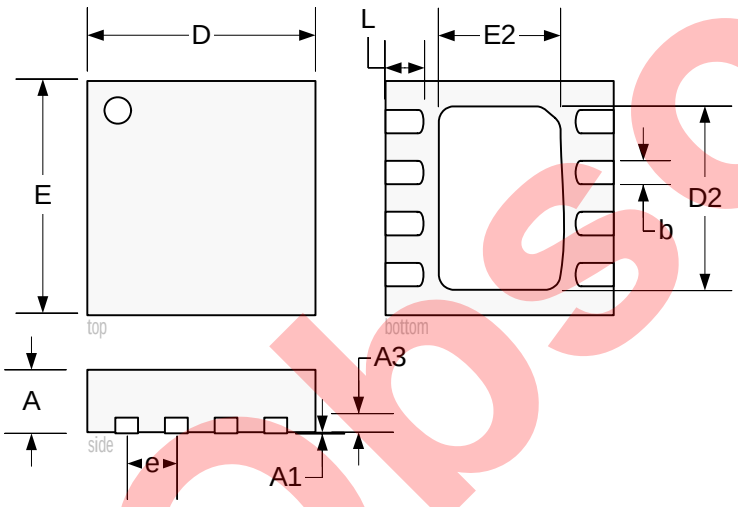
APPLICATION NOTE

LAYOUT GUIDELINES

The LX1800 is sensitive to noise at the reference pin so this node should be a low impedance path to ground for high frequency noise. As a precaution, the REF node should be routed away from digital switching traces. The Vcc Pin should be decoupled to ground with a 0.1µF ceramic capacitor located in close proximity to the IC.

PACKAGE DIMENSIONS

LD 8 Pin Plastic MLP Dual Exposed Pad



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.0315	0.0394
A1	0	0.05	0	0.0019
A3	0.20 REF		0.0079 REF	
b	0.25	0.30	0.010	0.0118
D	3.00 BSC		0.1181 BSC	
D2	1.60	2.50	0.0630	0.0984
e	0.65 BSC		0.0260 BSC	
E	3.00 BSC		0.1181 BSC	
E2	1.35	1.75	0.0531	0.0689
L	0.30	0.50	0.0071	0.0197

Note:

1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.

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NOTES